We Claim:

1. A detector array formed on a semiconductor material having a first side and a second side, the detector array comprising:

an entrance window formed on the first side, the entrance window being used to receive radiation; and

an array of detectors formed on the second side, one or more of the detectors being used for detecting the radiation received via the entrance window,

wherein the entrance window forms a junction with the semiconductor material, and the detectors comprise pixelated ohmic contacts.

2. The detector array of claim 1, wherein one or more detectors are surrounded by one or more junction separation implants, the junction separation implants surrounding the detectors in a form of a grid or rings.

3. The detector array of claim 1, wherein the entrance window is coupled to one selected from a group consisting of a scintillator, a scintillator array, a light guide or a diffuser for providing the radiation to the detector array via the entrance window.

4. The detector array of claim 1, wherein one or more detectors are coupled to readout electronics.

5. The detector array of claim 2, wherein the semiconductor material is high resistivity n-type silicon, the entrance window is p+ type, the array of detectors are n+ type, and the junction separation implants are p+ type.

6. The detector array of claim 2, wherein the semiconductor material is high resistivity p-type silicon, the entrance window is n+ type, the array of detectors are p+ type and the junction separation implants are n+ type.

7. The detector array of claim 1, wherein the array of detectors comprise radiation hardened detectors, and is used to detect at least one radiation selected from a group consisting of particles, light, x-ray, and gamma-ray.

8. The detector array of claim 1, wherein both the entrance window and the junction separation implants are reverse biased, and the reverse biasing generates in the semiconductor material a first depletion region originating at the first side and a plurality of second depletion regions originating at the second side with a pinch off region formed between the first depletion region and at least one of the second depletion regions.

9. The detector array of claim 1, wherein the entrance window is reverse biased with sufficiently high voltage so as to achieve a controlled avalanche effect.

10. The detector array of claim 9, wherein electric field at a periphery of the junction between the entrance window and the semiconductor material is shaped for preventing premature surface breakdown.

11. The detector array of claim 10, wherein the electric field is shaped for preventing premature surface breakdown by removing material from the semiconductor

material at the edge of the detector array so as to produce a beveled edge structure.

12. The detector array of claim 10, wherein the electric field is shaped for preventing premature breakdown by using guard rings or field plates.

13. The detector array of claim 1, wherein the grid surrounding the detectors comprises an inner grid surrounding one or more detectors and an outer grid surrounding the inner grid, wherein a first pixel size is achieved by biasing the inner grid and a second pixel size is achieved by biasing the outer grid, wherein the second pixel size is larger than the first pixel size.

14. The detector array of claim 1, wherein the entrance window is coupled with a CsI(Tl) scintillator.

15. The detector array of claim 14, wherein the entrance window is directly coupled with the CsI(Tl) scintillator.

16. The detector array of claim 14, wherein the entrance window is coupled with the CsI(Tl) scintillator via an interface that functions as a light guide between the entrance window and the CsI(Tl) scintillator.

17. The detector array of claim 1, wherein the entrance window is coupled with one selected from a group consisting of $CdWO_4$, NaI(Tl), LSO and BGO scintillators.

18. The detector array of claim 1, wherein the entrance window is directly coupled with one selected from the group consisting of $CdWO_4$, NaI(Tl), LSO and BGO scintillators.

19. The detector array of claim 1, wherein the entrance window is coupled with one selected from a group consisting of $CdWO_4$, NaI(Tl), LSO and BGO scintillators via an interface that functions as a light guide between the entrance window and the selected one of the scintillators.

20. The detector array of claim 1, wherein the entrance window is optimized for receiving light from a CsI(Tl) scintillator.

21. The detector array of claim 1, wherein the entrance window is optimized for receiving light from one selected from a group consisting of light from $CdWO_4$, NaI(Tl), LSO, BGO scintillators.

22. A method of forming a detector array on a semiconductor material having a first side and a second side, the method comprising the steps of:

forming an entrance window on the first side, the entrance window is for receiving radiation; and

forming an array of detectors on the second side, one or more of the detectors are used for detecting the radiation received via the entrance window,

wherein the entrance window forms a junction with the semiconductor material, and the detectors comprise pixelated ohmic contacts.

23. The method of forming a detector array of claim 22, the method further comprising the step of:

forming one or more junction separation implants, the junction separation implants surrounding the detectors in a form of a grid or rings.

24. The method of forming a detector array of claim 22, the method further comprising the step of:

coupling the entrance window to one selected from a group consisting of a scintillator, a scintillator array, a light guide or a diffuser for providing the radiation to the detector array via the entrance window.

25. The method of forming a detector array of claim 22, the method further comprising the step of:

coupling one or more detectors to readout electronics.

26. The method of forming a detector array of claim 22, the method further comprising the steps of:

reverse biasing the entrance window; and

reverse biasing the junction separation implants,

wherein the reverse biasing generates a plurality of depletion regions in the semiconductor material with a pinch off region between at least one of the depletion regions located between the pinch off region and the first side and the rest of the depletion regions located between the pinch off region and the second side.

27. The method of forming a detector array of claim 22, the method further comprising the step of:

reverse biasing the entrance window with sufficiently high voltage so as to achieve a controlled avalanche effect.

28. The method of forming a detector array of claim 25, the method further comprising the step of:

shaping electric field at a periphery of the junction between the entrance window and the semiconductor material to prevent premature surface breakdown.

29. The method of forming a detector array of claim 28, wherein the shape of the electric field is that of a beveled edge structure, wherein the beveled edge structure for the electric field is generated through removing material from the semiconductor material at the edge of the detector array in a shape of the beveled edge structure.

30. The method of forming a detector array of claim 28, wherein the shape of the electric field is that of a beveled edge structure, wherein the beveled edge structure for the electric field is generated using guard rings or field plates.

31. The method of forming a detector array of claim 22, wherein the grid surrounding the detectors comprises an inner grid surrounding one or more detectors and an outer grid surrounding the inner grid, wherein a first pixel size is achieved by biasing the inner grid and a second pixel size is achieved by biasing the outer grid, wherein the second pixel size is larger than the first pixel size.

32. A composite detector array comprising a plurality of detector arrays, wherein at least one of the detector arrays includes a detector array formed on a semiconductor material having a first side and a second side, the detector array comprising:

an entrance window formed on the first side, the entrance window being used to receive radiation; and

an array of detectors formed on the second side, one or more of the detectors being used to detect the radiation received via the entrance window,

wherein the entrance window forms a junction with the semiconductor material, and the detectors comprise pixelated ohmic contacts.

33. A detector array formed on a semiconductor material having a first side and a second side, the detector array comprising:

entrance window means formed on the first side, the entrance window means being used for receiving radiation; and

an array of detector means formed on the second side, one or more of the detector means being used for detecting the radiation received via the entrance window means,

wherein the entrance window means form a junction with the semiconductor material, and the detector means comprise pixelated ohmic contacts.